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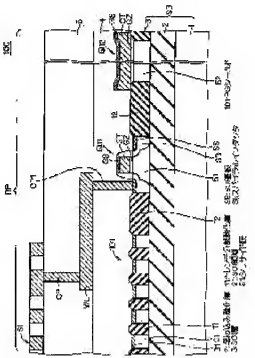
(54) SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING IT

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a semiconductor device having an inductor, by which an electrostatic induction loss and an electromagnetic induction loss can be reduced and that its structure and manufacturing process are prevented from becoming complicated.

SOLUTION: In a RF circuit part RP, a region corresponding to an arranging region of a spiral inductor SI in a SOI layer 3 is divided by means of a plurality of trench isolation oxide films 11, and a plurality of SOI regions 21 are formed. The trench isolation oxide films 11 are formed by embedding silicon oxide film in the trenches that are arranged so as to reach to the surface of a embedded oxide film 2 from the surface of the SOI layer 3. Each SOI region 21 is completely electrically separated. In addition, the trench isolation oxide films 11 have the shape extending approximately in a direction perpendicular to the surface of the embedded oxide film 2 with a given formation width.



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[Claim(s)]

[Claim 1]A semiconductor device comprising:

A semiconductor substrate.

A shield layer allocated in the principal surface of said semiconductor substrate.

At least one conductive part provided with an inductance element allocated on both sides of an interlayer insulation film in between on a formation area of said shield layer by which said shield layer was connected to earth potentials.

At least one current cutoff part which intercepts a course of an eddy current induced by said inductance element in said at least one plane of a conductive part.

[Claim 2]Are a SOI substrate characterized by comprising the following, and, [said at least one current cutoff part] The semiconductor device according to claim 1 with which said at least one conductive part includes two or more SOI areas electrically separated with said two or more isolation oxide films including two or more isolation oxide films which penetrate said SOI layer from the surface of said SOI layer, and reach said embedded oxide film, and which were allocated alternatively.

A board part from which said semiconductor substrate serves as a foundation.

An embedded oxide film allocated on this board part.

A SOI layer allocated on this embedded oxide film.

[Claim 3]The semiconductor device according to claim 2 which each of two or more of said isolation oxide films is predetermined formation width, and extends almost perpendicularly to the surface of said embedded oxide film.

[Claim 4]The 1st portion into which each of two or more of said isolation oxide films extends almost perpendicularly to the surface of said embedded oxide film in the 1st formation width, The semiconductor device according to claim 2 which comprises the 2nd portion that extends almost perpendicularly to the surface of said embedded oxide film in the 2nd formation width narrower than said 1st formation width succeeding the lower part of this 1st portion.

[Claim 5]Are a SOI substrate characterized by comprising the following, and, [said at least one conductive part] The semiconductor device according to claim 1 containing an insulating layer allocated including two

or more SOI areas which made said SOI layer thin and became prescribed thickness so that said at least one current cutoff part might fill between said two or more SOI areas at least.
A board part from which said semiconductor substrate serves as a foundation.
An embedded oxide film allocated on this board part.
A SOI layer allocated on this embedded oxide film.

[Claim 6]The semiconductor device according to claim 5 with which each of two or more of said SOI areas has semiconductor impurities in high concentration comparatively.
[Claim 7]The semiconductor device according to claim 5 with which each of two or more of said SOI areas has a silicide film on the upper surface.
[Claim 8]A board part from which said semiconductor substrate serves as a foundation, and an embedded oxide film allocated on this board part, Are a SOI layer allocated on this embedded oxide film a SOI substrate which it has, and, [said shield layer] Have two or more 1st SOI areas of the 1st conductivity type, and two or more 2nd SOI areas of the 2nd conductivity type, and, [said two or more 1st and 2nd SOI areas] With the combination, constitute two or more diodes and, [said at least one current cutoff part] The semiconductor device according to claim 1 with which it comprises at least one reverse bias diode with which reverse bias was impressed among said two or more diodes, and said at least one conductive part comprises a SOI area connected to earth potentials among said two or more 1st and 2nd SOI areas.
[Claim 9]The semiconductor device according to claim 8 which said two or more 1st and 2nd SOI areas are allocated in a field which made said SOI layer thin and became prescribed thickness, and is further provided with a wrap isolation oxide film for said 1st [two or more / the] and the 2nd SOI area whole region.
[Claim 10]Said two or more 1st SOI areas The 1st field of the respectively almost same thickness as said SOI layer, The semiconductor device according to claim 8 which has the 2nd field that adjoined said 1st field and made said SOI layer thin, and said each of two or more 2nd SOI areas is the almost same thickness as said SOI layer, and is further provided with a wrap isolation oxide film for said 2nd field top.
[Claim 11]The semiconductor device according to claim 10 with which each of said 1st field of two or more of said 1st SOI areas and two or more of said 2nd SOI areas has a silicide film on the upper surface.
[Claim 12]Said each of two or more 1st SOI areas is said SOI layer fields of prescribed thickness made thin, and, [said two or more 2nd SOI areas] The semiconductor device according to claim 8 which all are the almost same thickness as said SOI layer, and said two or more 1st and 2nd SOI areas adjoin mutually, and is separately provided further with a wrap isolation oxide film for said two or more of said 1st SOI areas.
[Claim 13]The semiconductor device according to claim 12 with which each of two or more of said 2nd SOI areas has a silicide film on the upper surface.
[Claim 14]The semiconductor device according to claim 12 whose plane view shape of said shield layer plane view shape of two or more of said 2nd SOI areas is rectangular shape, and is the shape which said two or more 2nd SOI areas sandwiched said isolation oxide film between each, and was allocated in the shape of a matrix.
[Claim 15]The semiconductor device according to claim 12 electrically connected by gate wire of the structure as a gate electrode of an MOS transistor where said two or more 2nd SOI areas are the same.
[Claim 16]The semiconductor device according to claim 8 with which said two or more 1st and 2nd SOI areas are allocated by turns, respectively, and gate structure of an MOS transistor is allocated on said two

or more 1st SOI areas.

[Claim 17]Said two or more 1st and 2nd SOI areas are allocated by turns, respectively, and said two or more 1st SOI areas, respectively The 1st field, The semiconductor device according to claim 8 which has the 2nd field contiguous to said 1st field and with which gate structure of an MOS transistor is allocated on said each 2nd field.

[Claim 18]The semiconductor device comprising according to claim 8:

Said two or more 1st and 2nd SOI areas are allocated by turns, respectively, and said two or more 1st SOI areas are the 1st field, respectively.

A silicide film which has the 2nd field contiguous to said 1st field, and was alternatively formed on said two or more 2nd SOI areas and said each 1st field so that it might not engage with said 2nd field.

[Claim 19]The semiconductor device according to claim 8 which said two or more 1st and 2nd SOI areas are allocated by turns, respectively, and has the silicide film alternatively formed on said two or more 1st SOI areas so that it might not engage with said two or more 2nd SOI areas.

[Claim 20]Are a SOI substrate characterized by comprising the following, and, [said board part] The semiconductor device according to claim 1 which has at least one hollow part to a field corresponding to a formation area of said inductance element, is constituted at least, and is provided with an eddy current inhibition part which controls generating of an eddy current induced by said inductance element.

A board part from which said semiconductor substrate serves as a foundation.

An embedded oxide film allocated on this board part.

A SOI layer allocated on this embedded oxide film.

[Claim 21]The semiconductor device according to claim 20 which comprises a hollow part with said eddy current inhibition part comparable as the length of a plane direction of said inductance element which is, carries out, has the about 1/10 depth, and has a spread of a plane direction comparable as a formation area of said inductance element at least.

[Claim 22]The semiconductor device according to claim 20 which comprises a porous layer with said eddy current inhibition part comparable as the length of a plane direction of said inductance element which is, carries out, has the about 1/10 depth, and has a spread of a plane direction comparable as a formation area of said inductance element at least.

[Claim 23]Are a SOI substrate characterized by comprising the following, and, [said SOI layer] The semiconductor device according to claim 1 provided with a porous layer comparable as the length of a plane direction of said inductance element which is, carries out, has the about 1/10 depth, and has a spread of a plane direction comparable as a formation area of said inductance element at least.

A board part from which said semiconductor substrate serves as a foundation.

An embedded oxide film allocated on this board part.

A SOI layer allocated on this embedded oxide film.

[Claim 24][said semiconductor substrate] [a field corresponding to a formation area of said inductance element] The semiconductor device according to claim 1 provided with a porous layer comparable as the length of a plane direction of said inductance element which is, carries out, has the about 1/10 depth, and

has a spread of a plane direction comparable as a formation area of said inductance element at least.
[Claim 25]The semiconductor device according to any one of claims 22 to 24 containing any of two or more holes or two or more trenches when it was formed by etching, or two or more holes which were formed by an anodization method said porous layer is.
[Claim 26]The semiconductor device according to claim 1 which is allocated by the lower part of two or more of said isolation oxide films, penetrates said embedded oxide film, and has further two or more trenches which reach in said board part.
[Claim 27]The semiconductor device according to claim 5 which is allocated by the lower part of said insulating layer allocated among said two or more SOI areas, penetrates said embedded oxide film, and has further two or more trenches which reach in said board part.
[Claim 28]Said at least one current cutoff part including two or more isolation oxide films which were missing from a prescribed depth and were allocated from the surface of said semiconductor substrate, [said at least one conductive part] The semiconductor device according to claim 1 which is allocated by the lower part of two or more of said isolation oxide films, and has further two or more trenches which reach a prescribed depth in said semiconductor substrate including two or more substrate regions classified with said two or more isolation oxide films.
[Claim 29]The semiconductor device according to claim 25 which is in a state with said two or more holes or an inside of two or more trenches near a vacuum.
[Claim 30]The semiconductor device according to any one of claims 26 to 28 which is in a state with an inside near a vacuum of said two or more trenches.
[Claim 31]A semiconductor device comprising:
A semiconductor substrate.
Two or more conductive parts which it had a shield layer allocated in the principal surface of said semiconductor substrate along arranged directions of this wiring layer by lower layer of a wiring layer, and said shield layer opened a gap, was allocated along arranged directions of said wiring layer, and were connected to earth potentials.
Two or more insulating parts allocated among said two or more conductive parts.

[Claim 32]The semiconductor device according to claim 31 with which said two or more conductive parts carry out two or more owners of a conductor film laminated by turns and the insulating layer, respectively.
[Claim 33]A manufacturing method of a semiconductor device provided with an inductance element characterized by comprising the following.
(a) A process for which a SOI substrate provided with a SOI layer allocated on an embedded oxide film allocated on a board part used as a foundation and this board part and a this embedded oxide film to carry out is prepared.
(b) A process of forming an opening which penetrates said SOI layer and said embedded oxide film at least, and reaches said board part, (c) A process of pouring in KOH solution from said opening, etching said board part, and forming a hollow part comparable as the length of a plane direction of said inductance element which is, carries out, has the about 1/10 depth, and has a spread of a plane direction comparable as a formation area of said inductance element at least.

[Claim 34]A manufacturing method of a semiconductor device provided with an inductance element characterized by comprising the following.
(a) A process of preparing the 1st silicon substrate and forming a porous layer comparable as the length of a plane direction of said inductance element which is, carries out, has the about 1/10 depth, and has a spread of a plane direction comparable as a formation area of said inductance element at least in the principal surface.
(b) A process of preparing the 2nd silicon substrate and forming silicon oxide on the principal surface of this 2nd silicon substrate.
(c) The principal surface in which said porous layer of said 1st silicon substrate was formed.
So that said silicon oxide of said 2nd silicon substrate may meet, A process of pasting said 1st and 2nd substrates together, making said 1st silicon substrate a board part, using said silicon oxide as an embedded oxide film, making thickness of said 2nd silicon substrate thin by the given thickness by polish, and forming a SOI layer, (d) A process of forming said inductance element in the upper part of a formation area of said porous layer.

[Claim 35]A manufacturing method of a semiconductor device provided with an inductance element characterized by comprising the following.
(a) A process of preparing the 1st silicon substrate and forming silicon oxide on the principal surface of this 1st silicon substrate.
(b) A process of preparing the 2nd silicon substrate and forming a porous layer comparable as the length of a plane direction of said inductance element which is, carries out, has the about 1/10 depth, and has a spread of a plane direction comparable as a formation area of said inductance element at least in the principal surface.
(c) Said silicon oxide of said 1st silicon substrate.
So that the principal surface in which said porous layer of said 2nd silicon substrate was formed may meet, Paste said 1st and 2nd substrates together, make said 1st silicon substrate into a board part, use said silicon oxide as an embedded oxide film, and thickness of said 2nd silicon substrate is made thin by the given thickness by polish, A process made into a SOI layer together with said porous layer, and a process of forming said inductance element in the upper part of a formation area of the (d) aforementioned porous layer.

[Claim 36]A manufacturing method of the semiconductor device according to claim 34 or 35 characterized by comprising the following.
A process of said process (a) forming two or more hole or two or more trenches by etching in the principal surface of said (a-1) 1st silicon substrate, and constituting said porous layer.
(a-2) A process of covering an opening of said two or more holes or two or more trenches by an insulating layer, and making the inside into hollow shape.

[Claim 37]A manufacturing method of the semiconductor device according to claim 34 or 35 characterized by comprising the following.
A process of said process (a) forming two or more hole or two or more trenches by etching in the principal

surface of said (a-1) 1st silicon substrate, and constituting said porous layer.
(a-2) A process of carrying out reduction removal of the opening of said two or more holes or two or more trenches by an annealing in inside of a hydrogen atmosphere, and making the inside into hollow shape.

[Claim 38]A manufacturing method of the semiconductor device according to claim 34 or 35 characterized by comprising the following.
A process of said process (a) forming two or more holes with anodic oxidation coating in the principal surface of said (a-1) 1st silicon substrate, and constituting said porous layer.
(a-2) A process of covering an opening of two or more of said holes by an insulating layer, and making the inside into hollow shape.

[Claim 39]A manufacturing method of the semiconductor device according to claim 34 or 35 characterized by comprising the following.
A process of said process (a) forming two or more holes from anodic oxidation coating in the principal surface of said (a-1) 1st silicon substrate, and constituting said porous layer.
(a-2) A process of carrying out reduction removal of the opening of two or more of said holes by an annealing in inside of a hydrogen atmosphere, and making the inside into hollow shape.

[Detailed Description of the Invention]
[0001]
[Field of the Invention]Especially this invention relates to the semiconductor device provided with the high frequency circuit with an inductor about a semiconductor device and a manufacturing method for the same.
[0002]
[Description of the Prior Art]An example of the composition of the semiconductor device provided with the high frequency circuit is explained using drawing 68. Drawing 68 is a block diagram showing the composition of the semiconductor device 90 with the function which receives the radio wave signal of a radio frequency (10 kHz - 100 GHz), and is outputted as a sound signal.
[0003]As shown in drawing 68, [the semiconductor device 90] It has the memory cell portion 93 which memorizes data required for the signal conditioning in RF circuit section 91 which restores to the received radio wave signal, the logic section 92 which processes the signal to which it restored by RF circuit section 91, and is changed into a sound signal, RF circuit section 91, and the logic section 92 at least. The semiconductor device 90 is connected to the sound emission device 95 which outputs the antenna system 94 and sound signal which detect a radio wave signal.
[0004]In what is called a high frequency circuit, it has **** by the inductor (inductance element) other than resistance or a capacitor including RF circuit section 91. Since an inductor acts so that a phase may be sped up to high frequency current, matching of high frequency current can be taken by using it against the capacitor which acts so that a phase may be delayed to high frequency current.
[0005]Although the inductor L1 in RF circuit section 91 is shown in drawing 68, the inductor L1 has the

parasitism capacitor C1, and the parasitism capacitor C1 is grounded via the resistance R1. Here, the resistance R1 is resistance of the semiconductor substrate which forms RF circuit section 91, when this resistance is very low or very high, it does not become a problem, but there are some which have the resistance (for example, 10-ohmcm grade) which consumes electric power by electrostatic induction loss depending on the kind of substrate.

[0006]The composition for preventing such an electrostatic induction loss is shown in drawing 69. In drawing 69, the parasitism capacitor C1 is not only grounded via the resistance R1, but has composition grounded via the resistance R2. Compared with the resistance R1, resistance is set up extremely low, high frequency current flows into grounding mainly via the resistance R2, and this resistance R2 does not cause an electrostatic induction loss.

[0007]the end A of the inductor L1 is connected to the antenna system 94 side, and the end B is connected to the source drain electrode of MOS transistor Q1 -- although carried out, this is an example of inductor connection.

[0008]The resistance R2 is a conductor board called a shield plate, and is allocated in the lower layer of the inductor L1. A perspective view shows the composition of the inductor L1 and a shield plate to drawing 70.

[0009]As shown in drawing 70, since the inductor L1 coils wiring spirally, carries out a time and is formed, in future explanation, it calls spiral inductor SI. The central part of the whirlpool which is one end of spiral inductor SI is connected to the lower layer wiring WL via contact part CP which penetrates the interlayer insulation film which is not illustrated. The wiring WL is allocated on the wrap interlayer insulation film SZ in the semiconductor substrate SB top.

[0010]The wiring WL corresponds to the end B of the inductor L1 shown in drawing 69, and the end A is equivalent to the end of another side of spiral inductor SI.

[0011]The semiconductor substrate SB is a silicon-on-insulator (silicon on insulator) board, and shows only the isolation oxide film FZ allocated into SOI layer SL and SOI layer SL in drawing 70. On the isolation oxide film FZ, tabular shield plate SP who has an area equivalent to the allocation area of the plane direction of spiral inductor SI at least in the position corresponding to the formation area of spiral inductor SI is allocated.

[0012]Shield plate SP comprises a conductor of the same low resistance as a wiring material, and since it is grounded via the wiring which is not illustrated, he does not cause an electrostatic induction loss.

[0013]However, since an eddy current occurs inside shield plate SP and an electromagnetic induction loss increases by the current which flows into spiral inductor SI, there is a new problem that total power loss increases rather.

[0014]In order to solve this problem, the par FOREITEDDO grand shield (it is called PG shield after perforated groundshield:) which cut the shield plate with every place and lacked it so that the course of an eddy current might be intercepted is proposed.

[0015]An example of PG shield is shown in drawing 71. PG shield shown in drawing 71 is constituted by two or more plate PL, and it is electrically insulated between each plate PL. The plane shape of plate PL is a triangle, and it is radiately allocated so that each vertex may constitute the central part of PG shield.

[0016]By taking such composition, the course of an eddy current is intercepted and an electromagnetic induction loss can be reduced.

[0017]

[Problem to be solved by the invention]Thus, although it is using PG shield in the conventional semiconductor device with an inductor and the electrostatic induction loss and the electromagnetic induction loss were reduced, While one layer of conductor layers needed to be increased to form PG shield and structure became complicated, there was a problem that a manufacturing process increased.

[0018]It was made in order that this invention might cancel the above problems, and it aims at providing the semiconductor device which prevented structure and a manufacturing process from becoming complicated while being able to reduce an electrostatic induction loss and an electromagnetic induction loss in a semiconductor device with an inductor.

[0019]

[Means for solving problem]The semiconductor device according to claim 1 concerning this invention is provided with the following.

A semiconductor substrate.

A shield layer allocated in the principal surface of said semiconductor substrate.

At least one conductive part provided with an inductance element allocated on both sides of an interlayer insulation film in between on a formation area of said shield layer by which said shield layer was connected to earth potentials.

At least one current cutoff part which intercepts a course of an eddy current in which this few **** is induced by said inductance element in one plane of a conductive part.

[0020]A board part from which, as for the semiconductor device according to claim 2 concerning this invention, said semiconductor substrate serves as a foundation, Are an embedded oxide film allocated on this board part, and a SOI layer allocated on this embedded oxide film a SOI substrate which it has, and, [said at least one current cutoff part] Said at least one conductive part includes two or more SOI areas electrically separated with said two or more isolation oxide films including two or more isolation oxide films which penetrate said SOI layer from the surface of said SOI layer, and reach said embedded oxide film and which were allocated alternatively.

[0021]Each of two or more of said isolation oxide films is predetermined formation width, and the semiconductor device according to claim 3 concerning this invention has extended almost perpendicularly to the surface of said embedded oxide film.

[0022]The 1st portion into which, as for the semiconductor device according to claim 4 concerning this invention, each of two or more of said isolation oxide films extends almost perpendicularly to the surface of said embedded oxide film in the 1st formation width, It comprises the 2nd portion that extends almost perpendicularly to the surface of said embedded oxide film in the 2nd formation width narrower than said 1st formation width succeeding the lower part of this 1st portion.

[0023]A board part from which, as for the semiconductor device according to claim 5 concerning this invention, said semiconductor substrate serves as a foundation, Are an embedded oxide film allocated on this board part, and a SOI layer allocated on this embedded oxide film a SOI substrate which it has, and, [said at least one conductive part] Including two or more SOI areas which made said SOI layer thin and became prescribed thickness, said at least one current cutoff part is allocated so that between said two or more SOI areas may be filled at least.

[0024]As for the semiconductor device according to claim 6 concerning this invention, each of two or more of

said SOI areas has semiconductor impurities in high concentration comparatively.

[0025]As for the semiconductor device according to claim 7 concerning this invention, each of two or more of said SOI areas has a silicide film on the upper surface.

[0026]The semiconductor device according to claim 8 concerning this invention, [said semiconductor substrate] Are a board part used as a foundation, an embedded oxide film allocated on this board part, and a SOI layer allocated on this embedded oxide film a SOI substrate which it has, and, [said shield layer] Have two or more 1st SOI areas of the 1st conductivity type, and two or more 2nd SOI areas of the 2nd conductivity type, and, [said two or more 1st and 2nd SOI areas] With the combination, constitute two or more diodes and, [said at least one current cutoff part] Comprising at least one reverse bias diode with which reverse bias was impressed among said two or more diodes, said at least one conductive part comprises a SOI area connected to earth potentials among said two or more 1st and 2nd SOI areas.

[0027]Said two or more 1st and 2nd SOI areas were allocated in the field which made said SOI layer thin and became prescribed thickness, and the semiconductor device according to claim 9 concerning this invention is further provided with the wrap isolation oxide film for said 1st [two or more / the] and the 2nd SOI area whole region.

[0028][the semiconductor device according to claim 10 concerning this invention] Said two or more 1st SOI areas The 1st field of the respectively almost same thickness as said SOI layer, It had the 2nd field that adjoined said 1st field and made said SOI layer thin, and said each of two or more 2nd SOI areas is the almost same thickness as said SOI layer, and is further provided with the wrap isolation oxide film for said 2nd field top.

[0029]As for the semiconductor device according to claim 11 concerning this invention, each of said 1st field of two or more of said 1st SOI areas and two or more of said 2nd SOI areas has a silicide film on the upper surface.

[0030][the semiconductor device according to claim 12 concerning this invention] Said each of two or more 1st SOI areas is said SOI layer fields of the prescribed thickness made thin, and, [said two or more 2nd SOI areas] All are the almost same thickness as said SOI layer, and said two or more 1st and 2nd SOI areas adjoined mutually, and are separately provided further with the wrap isolation oxide film for said two or more of said 1st SOI areas.

[0031]As for the semiconductor device according to claim 13 concerning this invention, each of two or more of said 2nd SOI areas has a silicide film on the upper surface.

[0032]Plane view shape of two or more of said 2nd SOI areas of the semiconductor device according to claim 14 concerning this invention is rectangular shape, and plane view shape of said shield layer is the shape which said two or more 2nd SOI areas sandwiched said isolation oxide film between each, and was allocated in the shape of a matrix.

[0033]The semiconductor device according to claim 15 concerning this invention is electrically connected by gate wire of the structure as a gate electrode of an MOS transistor where said two or more 2nd SOI areas are the same.

[0034]Said two or more 1st and 2nd SOI areas are allocated by turns, respectively, and, as for the semiconductor device according to claim 16 concerning this invention, gate structure of an MOS transistor is allocated on said two or more 1st SOI areas.

[0035][the semiconductor device according to claim 17 concerning this invention] Said two or more 1st and

2nd SOI areas are allocated by turns, respectively, said two or more 1st SOI areas have the 1st field and the 2nd field contiguous to said 1st field, respectively, and gate structure of an MOS transistor is allocated on said each 2nd field.

[0036][the semiconductor device according to claim 18 concerning this invention] Said two or more 1st and 2nd SOI areas are allocated by turns, respectively, and said two or more 1st SOI areas, respectively The 1st field, It has the 2nd field contiguous to said 1st field, and has the silicide film alternatively formed on said two or more 2nd SOI areas and said each 1st field so that it might not engage with said 2nd field.

[0037]Said two or more 1st and 2nd SOI areas are allocated by turns, respectively, and the semiconductor device according to claim 19 concerning this invention has the silicide film alternatively formed on said two or more 1st SOI areas so that it might not engage with said two or more 2nd SOI areas.

[0038][the semiconductor device according to claim 20 concerning this invention] Said semiconductor substrate is the board part used as a foundation, the embedded oxide film allocated on this board part, and the SOI layer allocated on this embedded oxide film a SOI substrate which it has, and it, [said board part] At least, to the field corresponding to the formation area of said inductance element, it has at least one hollow part, was constituted, and has the eddy current inhibition part which controls generating of the eddy current induced by said inductance element.

[0039]The semiconductor device according to claim 21 concerning this invention comprises a hollow part with said eddy current inhibition part comparable as the length of a plane direction of said inductance element which is, carries out, has the about 1/10 depth, and has a spread of a plane direction comparable as a formation area of said inductance element at least.

[0040]The semiconductor device according to claim 22 concerning this invention comprises a porous layer with said eddy current inhibition part comparable as the length of a plane direction of said inductance element which is, carries out, has the about 1/10 depth, and has a spread of a plane direction comparable as a formation area of said inductance element at least.

[0041][the semiconductor device according to claim 23 concerning this invention] Said semiconductor substrate is a board part used as a foundation, an embedded oxide film allocated on this board part, and a SOI layer allocated on this embedded oxide film a SOI substrate which it has, and it, [said SOI layer] It can have a porous layer comparable as the length of a plane direction of said inductance element which is, carries out, has the about 1/10 depth, and has a spread of a plane direction comparable as a formation area of said inductance element at least.

[0042][the semiconductor device according to claim 24 concerning this invention] Said semiconductor substrate equips a field corresponding to a formation area of said inductance element with a porous layer comparable as the length of a plane direction of said inductance element which is, carries out, has the about 1/10 depth, and has a spread of a plane direction comparable as a formation area of said inductance element at least.

[0043]The semiconductor device according to claim 25 concerning this invention contains any of two or more holes in which said porous layer was formed by two or more holes or two or more trenches when it was formed by etching, or an anodization method they are.

[0044]The semiconductor device according to claim 26 concerning this invention is allocated by the lower part of two or more of said isolation oxide films, penetrates said embedded oxide film, and has further two or more trenches which reach in said board part.

[0045]The semiconductor device according to claim 27 concerning this invention is allocated by the lower part of said insulating layer allocated among said two or more SOI areas, penetrates said embedded oxide film, and has further two or more trenches which reach in said board part.
[0046][the semiconductor device according to claim 28 concerning this invention] Said at least one current cutoff part including two or more isolation oxide films which were missing from the prescribed depth and were allocated from the surface of said semiconductor substrate, [said at least one conductive part] Including two or more substrate regions classified with said two or more isolation oxide films, it is allocated by the lower part of two or more of said isolation oxide films, and has further two or more trenches which reach the prescribed depth in said semiconductor substrate.
[0047]The semiconductor device according to claim 29 concerning this invention is in a state with said two or more holes or the inside of two or more trenches near a vacuum.
[0048]The semiconductor device according to claim 30 concerning this invention is in a state with the inside near a vacuum of said two or more trenches.
[0049]The semiconductor device according to claim 31 concerning this invention is provided with the following.
Semiconductor substrate.
Two or more conductive parts which it had the shield layer allocated in the principal surface of said semiconductor substrate along the arranged directions of this wiring layer by the lower layer of the wiring layer, and said shield layer opened the gap, was allocated along the arranged directions of said wiring layer, and were connected to earth potentials.
Two or more insulating parts allocated among said two or more conductive parts.

[0050]The semiconductor device according to claim 32 concerning this invention is carrying out two or more owners of the conductor film and insulating layer by which said two or more conductive parts were laminated by turns, respectively.
[0051]The manufacturing method of the semiconductor device according to claim 33 concerning this invention is provided with the following.
The process for which a SOI substrate provided with the SOI layer allocated on the embedded oxide film allocated on the board part which is a manufacturing method of the semiconductor device provided with the inductance element, and serves as a foundation, and this board part, and the this embedded oxide film to carry out is prepared (a).
The process (b) of forming the opening which penetrates said SOI layer and said embedded oxide film at least, and reaches said board part.
The process (c) of pouring in KOH solution from said opening, etching said board part, and forming the hollow part comparable as the length of the plane direction of said inductance element which is, carries out, has the about 1/10 depth, and has a spread of a plane direction comparable as the formation area of said inductance element at least.

[0052]A manufacturing method of the semiconductor device according to claim 34 concerning this invention is provided with the following.
Are a manufacturing method of a semiconductor device provided with an inductance element, and the 1st

silicon substrate is prepared, A process of forming a porous layer comparable as the length of a plane direction of said inductance element which is, carries out, has the about 1/10 depth, and has a spread of a plane direction comparable as a formation area of said inductance element at least in the principal surface (a).
A process (b) of preparing the 2nd silicon substrate and forming silicon oxide on the principal surface of this 2nd silicon substrate.
The principal surface in which said porous layer of said 1st silicon substrate was formed.
So that said silicon oxide of said 2nd silicon substrate may meet, Paste said 1st and 2nd substrates together and said 1st silicon substrate is made into a board part, A process (c) of using said silicon oxide as an embedded oxide film, making thickness of said 2nd silicon substrate thin by the given thickness by polish, and forming a SOI layer, and a process (d) of forming said inductance element in the upper part of a formation area of said porous layer.

[0053]A manufacturing method of the semiconductor device according to claim 35 concerning this invention is provided with the following.
A process of being a manufacturing method of a semiconductor device provided with an inductance element, preparing the 1st silicon substrate, and forming silicon oxide on the principal surface of this 1st silicon substrate (a).
A process (b) of preparing the 2nd silicon substrate and forming a porous layer comparable as the length of a plane direction of said inductance element which is, carries out, has the about 1/10 depth, and has a spread of a plane direction comparable as a formation area of said inductance element at least in the principal surface.
Said silicon oxide of said 1st silicon substrate.
So that the principal surface in which said porous layer of said 2nd silicon substrate was formed may meet, Paste said 1st and 2nd substrates together, make said 1st silicon substrate into a board part, use said silicon oxide as an embedded oxide film, and thickness of said 2nd silicon substrate is made thin by the given thickness by polish, A process (c) made into a SOI layer together with said porous layer, and a process (d) of forming said inductance element in the upper part of a formation area of said porous layer.

[0054][the manufacturing method of the semiconductor device according to claim 36 concerning this invention] The process (a-1) of said process (a) forming two or more hole or two or more trenches by etching in the principal surface of said 1st silicon substrate, and constituting said porous layer, Covering the opening of said two or more holes or two or more trenches by an insulating layer, the inside includes the process (a-2) made into hollow shape.
[0055][the manufacturing method of the semiconductor device according to claim 37 concerning this invention] The process (a-1) of said process (a) forming two or more hole or two or more trenches by etching in the principal surface of said 1st silicon substrate, and constituting said porous layer, Carrying out reduction removal of the opening of said two or more holes or two or more trenches by the annealing in the inside of a hydrogen atmosphere, the inside includes the process (a-2) made into hollow shape.
[0056][the manufacturing method of the semiconductor device according to claim 38 concerning this invention] Covering the process (a-1) from which said process (a) forms two or more holes with anodic

oxidation coating in the principal surface of said 1st silicon substrate, and constitutes said porous layer, and the opening of two or more of said holes by an insulating layer, the inside includes the process (a-2) made into hollow shape.

[0057][the manufacturing method of the semiconductor device according to claim 39 concerning this invention] The process (a-1) of said process (a) forming two or more holes from anodic oxidation coating in the principal surface of said 1st silicon substrate, and constituting said porous layer, Carrying out reduction removal of the opening of two or more of said holes by the annealing in the inside of a hydrogen atmosphere, the inside includes the process (a-2) made into hollow shape.

[0058]

[Mode for carrying out the invention]As Embodiment 1 of the semiconductor device concerning <A. embodiment 1> <A-1. equipment configuration> this invention, the composition of the semiconductor device 100 is shown in drawing 1.

[0059]If the semiconductor device 90 explained using drawing 68 is taken for an example, the semiconductor device 100 shown in drawing 1 shows a part of RF circuit section 91, and shows it as RF circuit section RP.

[0060]In drawing 1, RF circuit section RP is allocated on SOI substrate SB which comprises the silicon substrate 1, the embedded oxide film 2 allocated on this silicon substrate 1, and SOI layer 3 allocated on the embedded oxide film 2.

[0061]In RF circuit section RP, a field corresponding to region disposing of spiral inductor SI (plane constitution is referring to drawing 70) of SOI layer 3 is divided by two or more trench isolation oxide films 11, and two or more SOI areas 21 are formed. The trench isolation oxide film 11 is formed by embedding silicon oxide in a trench allocated so that the surface of the embedded oxide film 2 might be arrived at from the surface of SOI layer 3, and each SOI area 21 is separated completely electrically.

[0062]The trench isolation oxide film 11 is predetermined formation width, and has the shape which extends almost perpendicularly to the surface of the embedded oxide film 2.

[0063]The silicide film 31 is allocated in the upper part of each SOI area 21, and the PG shield 101 (shield layer) is constituted by two or more trench isolation oxide films 11, SOI area 21, and the silicide film 31, respectively.

[0064]An isolation oxide film which specifies a SOI area separated completely electrically like the trench isolation oxide film 11 is called a complete isolation oxide film.

[0065]A formation area of the PG shield 101 is prescribed by the trench isolation oxide film 12, outside a formation area of the PG shield 101, with the trench isolation oxide film 12, SOI layer 3 is divided and SOI areas 51 and 52 are formed. The trench isolation oxide film 12 is a complete isolation oxide film, and SOI areas 51 and 52 are separated completely electrically.

[0066]MOS transistors Q11 and Q12 are formed in SOI areas 51 and 52, respectively. The gate dielectric film GZ in which both MOS transistors Q11 and Q12 were allocated on SOI area 51 and 52, It has silicide film GS allocated on gate electrode GT allocated on the gate dielectric film GZ, and gate electrode GT, and the sidewall insulating layer GW allocated so that those sides might be covered. MOS transistors Q11 and Q12 are general MOS transistors, and the composition and manufacturing method do not have the feature.

[0067]In MOS transistor Q11, although silicide film SS and the source drain area SD which were allocated in the surface of SOI area 51 of the outside of the sidewall insulating layer GW are shown, it cannot be

overemphasized that it has the same composition also in MOS transistor Q12. Since MOS transistor Q12 expresses the section composition in alignment with the longitudinal direction of gate electrode GT, above-mentioned composition is not only illustrated.

[0068]And the interlayer insulation film 4 which comprises silicon oxide is allocated, and the wiring WL which electrically connects spiral inductor SI to MOS transistor Q11 is allocated on the interlayer insulation film 4 so that the SOI substrate SB top whole region may be covered. One end of the wiring WL is connected to contact part CP1 which penetrates the interlayer insulation film 4 and reaches silicide film SS of MOS transistor Q11. Contact part CP1 embeds a conductor in the contact hole which penetrates the interlayer insulation film 4, and it is constituted.

[0069]The interlayer insulation film 5 which comprises silicon oxide is allocated, and spiral inductor SI is allocated on the interlayer insulation film 5 so that the interlayer insulation film 4 top may be covered. One end of spiral inductor SI is connected to the wiring WL via contact part CP which penetrates the interlayer insulation film 5 and reaches the wiring WL.

[0070]Here, plane view shape of the PG shield 101 is shown in drawing 2. As shown in drawing 2, plane view shape makes an abbreviated L character type, respectively, and, as for each SOI area 21 which constitutes the PG shield 101, each is allocated symmetrically.

[0071]That is, two or more SOI areas 21 are classified into SOI areas 21L and 21S of two kinds of analogue-like size, and SOI area 21S is allocated so that it may become the arrangement form same to a field (an inner area and a name) specified with two arms arms and SOI area 21L cross at right angles as SOI area 21L.

[0072]And if 1 set of SOI areas 21L and 21S is made into the 1st unit, it has composition that the 2nd unit was allocated by shape symmetrical with a line to the 1st unit, and also the 3rd and 4th units were allocated by shape symmetrical with a line to the 1st and 2nd units. Therefore, the PG shield 101 will have four SOI areas 21S and four SOI areas 21L.

[0073]And since one side of each 2 arm is allocated so that it may counter with one side of two arms of other SOI areas 21L, as for the plane view shape of the trench isolation oxide film 11 specified in four SOI areas 21L, four SOI areas 21L are making the cross type.

[0074][the composition of the PG shield 101 shown in drawing 1] for example, it corresponds to the section in the X-X line in drawing 2, and it will electrically be connected to predetermined wiring (not shown) via the contact part (not shown) which penetrates the interlayer insulation film 4 in drawing 1 and which carries out and reaches the silicide film 31, and each SOI area 21 will be grounded via the wiring concerned.

[0075]As more than the <A-2. operation effect> explained, the PG shield 101 comprises two or more SOI areas 21 electrically separated with the trench isolation oxide film 11, and a layered product of the silicide film 31, Since the course of an eddy current is intercepted with the trench isolation oxide film 11 while being able to reduce an electrostatic induction loss, since the layered product concerned serves as low resistance comparatively by existence of the silicide film 31, the electromagnetic induction loss resulting from an eddy current is not received.

[0076]Since the increase in an electrostatic induction loss and an electromagnetic induction loss decreases Q value (value which broke the energy stored in an inductor by various losses) showing the performance of an inductor, reducing an electrostatic induction loss and an electromagnetic induction loss will contribute to improvement in Q value.

[0077]In the formation process of the trench isolation oxide film 12 of the element formation region in which MOS transistor Q11 and Q12 grade are formed as for the trench isolation oxide film 11, For example, it can form by patterning SOI layer 3 simultaneously using a common resist mask, Since the silicide film 31 can be formed simultaneously with the silicide films GS and SS of MOS transistors Q11 and Q12, a process new for formation of the PG shield 101 does not increase, and a manufacturing method does not become complicated.

[0078]Since the PG shield 101 is formed in SOI layer 3, a conductor layer new for formation of PG shield is unnecessary, and device structure does not become complicated.

[0079]Although the composition which performs separation between elements using trench separation in the above explanation was shown, it cannot be overemphasized that the element separation art of others, such as LOCOS (Local Oxide of Silicon) separation and MESA separation, may be used. Also in embodiments other than the embodiment aiming at solution of dishing peculiar to trench separation among Embodiments 2-16 concerning this invention explained below, this is the same.

[0080]The plane view shape of a <A-3. modification> PG shield is not limited to the shape shown in drawing 2, and should just be provided with a notch section which intercepts the course of an eddy current.

[0081]Other examples of the plane view shape of PG shield are shown in drawing 3 - drawing 7.

[0082]Plane view shape PG shield shown in drawing 3, [triangular two SOI area 21A] Are allocated so that each base may counter, and the 1st unit is constituted, It has the composition that the 2nd unit was allocated by shape symmetrical with a line to the 1st unit, and also the 3rd and 4th units were allocated by shape symmetrical with a line to the 1st and 2nd units, and has eight SOI areas 21A. The trench isolation oxide film 11 is allocated between each SOI area 21A.

[0083]PG shield shown in drawing 4 is equal to a size of the whole PG shield, and plane view shape has composition with the notch section NP to which rectangular SOI area 21B reaches even the center section. The trench isolation oxide film 11 is allocated in the notch section NP, and an eddy current will be intercepted in the notch section NP.

[0084]Four rectangular SOI areas 21C are allocated in the shape of [two-line / of two rows] a matrix, and PG shield shown in drawing 5 is constituted. The trench isolation oxide film 11 is allocated between each SOI area 21C.

[0085]PG shield shown in drawing 6 is allocated in one row so that a neighborhood of the longitudinal direction may become parallel mutually in four elongated-shaped SOI areas 21D. The trench isolation oxide film 11 is allocated between each SOI area 21D.

[0086]PG shield shown in drawing 7 has L character type SOI areas 21L, 21M, and 21S of three kinds of analogue-like size, and rectangular SOI area 21E. And SOI area 21M is allocated so that it may become the arrangement form same to the inner area specified with two arms arms and SOI area 21L cross at right angles as SOI area 21L, SOI area 21S is allocated so that it may become SOI area 21M and the same arrangement form in the inner area specified with two arms arms and SOI area 21M cross at right angles, and SOI area 21E is allocated in the inner area specified with two arms arms and SOI area 21S cross at right angles. The trench isolation oxide film 11 is allocated between each SOI areas 21L, 21M, and 21S and 21E.

[0087]As Embodiment 2 of the semiconductor device concerning <B. embodiment 2> <B-1. equipment configuration> this invention, the composition of the semiconductor device 200 is shown in drawing 8.

[0088]If the semiconductor device 90 explained using drawing 68 is taken for an example, the semiconductor device 200 shown in drawing 8 shows a part of RF circuit section 91 and logic section 92, and shows it as RF circuit section RP and logic section LP gas, respectively.
[0089]In drawing 8, RF circuit section RP and logic section LP gas are allocated on SOI substrate SB which comprises the silicon substrate 1, the embedded oxide film 2 allocated on this silicon substrate 1, and SOI layer 3 allocated on the embedded oxide film 2.
[0090]In RF circuit section RP, a field corresponding to region disposing of spiral inductor SI (plane constitution is referring to drawing 70) of SOI layer 3 is divided by two or more trench isolation oxide films 13, and two or more SOI areas 22 are formed. The trench isolation oxide film 12 is formed by embedding silicon oxide in a trench allocated so that the surface of the embedded oxide film 2 might be arrived at from the surface of SOI layer 3, and each SOI area 22 is separated completely electrically.
[0091]The silicide film 32 is allocated in the upper part of each SOI area 22, and the PG shield 102 (shield layer) is constituted by two or more trench isolation oxide films 13, SOI area 22, and the silicide film 32, respectively.
[0092]The trench isolation oxide film 13 comprises the 1st portion that extends almost perpendicularly to the surface of the embedded oxide film 2 in the 1st formation width, and the 2nd portion that extends almost perpendicularly to the surface of the embedded oxide film 2 succeeding the lower part of the 1st portion in the 2nd formation width narrower than the 1st formation width.
[0093]Shape where it explained, for example using drawing 2 may be used for plane view shape of the PG shield 102, and shape where it explained using drawing 3 - drawing 7 may be used for it.
[0094]Between RF circuit section RP and logic section LP gas, it is electrically separated by the trench isolation oxide film 14, and in logic section LP gas, SOI layer 3 is divided and SOI areas 61 and 62 are formed with the trench isolation oxide film 15.
[0095]Like the trench isolation oxide film 15, a SOI area is not separated completely electrically but an isolation oxide film in which SOI layer 3 was allocated by the lower part as the well area WR is called a partial isolation oxide film.
[0096]A <B-1-1. partial isolation oxide film> Here, a partial isolation oxide film is explained briefly. In an MOS transistor electrically separated from other elements completely, latchup between other MOS transistors does not happen theoretically with a complete isolation oxide film.
[0097]Therefore, when a silicon-on-insulator device which has a CMOS transistor using a complete isolation oxide film was manufactured, there was a merit which can use the minimum separation width decided with ultra-fine processing technology, and can reduce a chip area. However, a channel forming region (body region) is covered with a carrier (NMOS hole) generated according to an ionization-by-collision phenomenon, It had the influence by a substrate floating effect of kink occurring by this, or pressure-proofing of operation deteriorating, and the frequency dependence of a time delay occurring, since potential of a channel forming region is not stabilized.
[0098][about change of potential of such a channel forming region] "IEEE TRANSACTIONSON ELECTRON DEVICES, VOL.45, NO.7, JULY 1998, pp1479-1484, "Analysis ofDelay Time Instability According It is concretely indicated to to the Operating Frequency in Field Shield Isolated silicon on insulator Circuits" S.Maeda et al." (literature 1). That is, since potential of a body region is changed transitionally, in connection with this, it changes transitionally, and I hear that the characteristics of a transistor also become

unstable and they have circuit operation (refer to drawing 7 of the literature 1).
[0099]It is also verified that frequency dependence appears in delay time as shown by drawing 5 of the literature 1.
[0100]Then, if the partial isolation oxide film called partial trench separation was devised and it takes the composition of drawing 8 for an example, Migration of a carrier is possible through the well area WR of the lower part of the trench isolation oxide film 15, Since a carrier can be prevented from a channel forming region being covered and the potential of a channel forming region can be fixed through the well area WR, various problems by a substrate floating effect do not occur.
[0101]Although the composition which used together the partial isolation oxide film and the complete isolation oxide film in drawing 8 is shown, it is indicated by drawing 4 - drawing 7 and drawing 8 - drawing 27 in the Description of the patent application number 11-177091 about an example of combined use and a manufacturing method for the same of a partial isolation oxide film and a complete isolation oxide film.
[0102]When using together a partial isolation oxide film and a complete isolation oxide film, one side of an isolation oxide film may serve as shape of a complete isolation oxide film, and the other side may use a merged isolation oxide film used as shape of a partial isolation oxide film, but. It is indicated by drawing 1 - drawing 38 in a Description of the patent application number 2000-39480 about composition of a merged isolation oxide film, and a manufacturing method for the same.
[0103][sectional shape / of a partial isolation oxide film] ""IEEE International. SOIConference, Oct.1999, pp131-132, "Bulk-Layout-Compatible 0.18 micrometer silicon on insulator-CMOS Technology Using Body-Fixed . It is shown using a SEM photograph as drawing 2 of Partial Trench Isolation(PIT)" Y.Hirano et al." (literature 2).
[0104]Here, it returns to explanation of drawing 8. In logic section LP gas of drawing 8, MOS transistors Q21 and Q22 are formed in SOI areas 61 and 62, respectively.
[0105]Since MOS transistors Q21 and Q22 are general MOS transistors as well as MOS transistors Q11 and Q12 shown in drawing 1 and their fundamental component is the same, About the same composition as MOS transistors Q11 and Q12, the same numerals are attached and the overlapping explanation is omitted.
[0106]In addition, about the same composition as the semiconductor device 100 shown in drawing 1, the same numerals are attached and the overlapping explanation is omitted.
[0107]The manufacturing method of the semiconductor device 200 is explained using a <B-2. manufacturing method> next drawing 9 in which a manufacturing process is shown in order - drawing 11.
[0108]First, after forming the silicon oxide OX about 20 nm thick and the silicon nitride film SN about 200 nm thick one by one on SOI layer 3 in a process which prepares SOI substrate SB and is shown in drawing 9, Using resist mask RM1 patterned, the silicon oxide OX, The silicon nitride film SN and a multilayer film of SOI layer 3 are etched so that a lower layer part of SOI layer 3 may remain, and trench TR131, TR141, and TR15 are formed in a field in which the trench isolation oxide films 13, 14, and 15 are formed.
[0109]Next, in a process shown in drawing 10, a part of trench TR131 and TR141, [wrap] The trenches TR13 and TR14 which penetrate SOI layer 3 are formed by etching further a portion which is not completely covered by trench TR131 and resist mask RM2 of TR141 using wrap resist mask RM2 in trench TR15.
[0110]Next, after removing resist mask RM2, cross to the whole surface and silicon oxide about 500 nm thick is formed, Embed the trenches TR13-TR15, and it grinds to the middle of the silicon nitride film SN by CMP (Chemical Mechanical Polishing) processing, Then, by removing the silicon nitride film SN and the

silicon oxide OX, as shown in drawing 11, the trench isolation oxide films 13-15 are obtained.

[0111]The semiconductor device 200 is obtained after this through the manufacturing process (the existing Salicide process is included) of the existing MOS transistor, the manufacturing process of an interlayer insulation film, the manufacturing process of a wiring layer, the manufacturing process of a spiral inductor, etc.

[0112]As more than the <B-3. operation effect> explained, the PG shield 102 comprises two or more SOI areas 22 electrically separated with the trench isolation oxide film 13, and a layered product of the silicide film 32, Since the course of an eddy current is intercepted with the trench isolation oxide film 13 while being able to reduce an electrostatic induction loss, since the layered product concerned serves as low resistance comparatively by existence of the silicide film 32, the electromagnetic induction loss by an eddy current is not received.

[0113]In a formation process of the trench isolation oxide film 15 in which the trench isolation oxide film 13 is used for separation with MOS transistors Q21 and Q22 of the trench isolation oxide film 14 of a boundary of logic section LP gas and RF circuit section RP, and logic section LP gas, Since it can form using the common resist masks RM1 and RM2 and the silicide film 32 can be formed simultaneously with the silicide films GS and SS of MOS transistors Q21 and Q22, A process new for formation of the PG shield 102 does not increase, and a manufacturing method does not become complicated.

[0114]There is the feature that shape of a top edge part of the trench isolation oxide film 13 can be made the same as shape of a top edge part of the trench isolation oxide films 14 and 15.

[0115]Since the PG shield 102 is formed in SOI layer 3, a conductor layer new for formation of PG shield is unnecessary, and device structure does not become complicated.

[0116]Since the trench isolation oxide film 15 which is a partial isolation oxide film separates between elements in logic section LP gas, Potential of a channel forming region (body region) can be fixed through the well area WR of the lower part of the trench isolation oxide film 15, and various problems by a substrate floating effect can be prevented.

[0117]Although the trench isolation oxide film 13 showed the example formed using the common resist masks RM1 and RM2 in the formation process of the trench isolation oxide film 14 and the trench isolation oxide film 15, [in the <B-4. modification> PG shield 102] [the trench isolation oxide film] If it is permissible that a process becomes a little complicated, it is good also as simple sectional shape like the trench isolation oxide film 11 of the semiconductor device 100 explained using drawing 1.

[0118]As Embodiment 3 of the semiconductor device concerning <C. embodiment 3> <C-1. equipment configuration> this invention, the composition of the semiconductor device 300 is shown in drawing 12.

[0119]The semiconductor device 300 shown in drawing 12 shows the composition in which RF circuit section RP and logic section LP gas were allocated on SOI substrate SB like the semiconductor device 200 shown in drawing 8.

[0120]In RF circuit section RP, two or more independent SOI areas 23 are formed on the embedded oxide film 2 corresponding to region disposing of spiral inductor SI (plane constitution is referring to drawing 70), and the PG shield 103 (shield layer) is constituted. And as for the PG shield 103, the whole is covered with the trench isolation oxide film 16.

[0121]Shape where it explained, for example using drawing 2 may be used for plane view shape of the PG shield 103, and shape where it explained using drawing 3 - drawing 7 may be used for it.

[0122]In logic section LP gas, with the trench isolation oxide film 15 which is a partial isolation oxide film, SOI layer 3 is divided and SOI areas 71 and 72 are formed. And MOS transistors Q31 and Q32 are formed in SOI areas 71 and 72, respectively.

[0123]Since MOS transistors Q31 and Q32 are general MOS transistors as well as MOS transistors Q11 and Q12 shown in drawing 1 and their fundamental component is the same, About the same composition as MOS transistors Q11 and Q12, the same numerals are attached and the overlapping explanation is omitted.

[0124]In addition, about the same composition as the semiconductor device 100 shown in drawing 1, the same numerals are attached and the overlapping explanation is omitted.

[0125]If SOI area 23 is explained using drawing 10 in which the manufacturing method of the semiconductor device 200 is shown, in RF circuit section RP, it will form trench TR14 which etches further the portion which is not covered by resist mask RM2 of trench TR141, and penetrates SOI layer 3. Then, while removing resist mask RM2 and removing completely silicon oxide OX and the silicon nitride film SN, it can form by removing a part of SOI layer 3. It will cover with a resist mask so that silicon oxide OX and the silicon nitride film SN may not be removed in logic section LP gas in this case.

[0126]And while after formation of SOI area 23 removing the resist mask of logic section LP gas, and crossing it to the whole surface, forming silicon oxide and embedding trench TR15, The trench formed when forming SOI area 23 is embedded, it grinds to the middle of the silicon nitride film SN which remains in logic section LP gas by CMP treatment, and the trench isolation oxide films 16 and 15 are obtained by removing the silicon nitride film SN and the silicon oxide OX after that.

[0127]SOI area 23 is a field equivalent to the so-called base of a body region, and the thickness becomes equal to the thickness of the well area WR of the lower part of the trench isolation oxide film 15.

[0128]Since the PG shield 103 comprises independent SOI area 23 of the plurality covered with the trench isolation oxide film 16 as more than the <C-2. operation effect> explained, Since the course of an eddy current is intercepted with the trench isolation oxide film 16 while being able to reduce an electrostatic induction loss, the electromagnetic induction loss by an eddy current is not received.

[0129]Since the PG shield 103 divides SOI layer 3 and is formed, a conductor layer new for formation of PG shield is unnecessary, and device structure does not become complicated.

[0130]Since the trench isolation oxide film 15 which is a partial isolation oxide film separates between elements in logic section LP gas, The potential of a channel forming region (body region) can be fixed through the well area WR of the lower part of the trench isolation oxide film 15, and various problems by a substrate floating effect can be prevented.

[0131]The PG shield 103 which beyond the <C-3. modification 1> explained comprises two or more independent SOI areas 23. this -- SOI layer 3 -- a well -- SOI area 23 being used as a conductor, since pouring (or called channel pouring) is performed, and it is low resistance rather than the silicon substrate 1, but. What is necessary is just to pour impurities into SOI area 23 comparatively at high concentration to lower resistance. An example of the process is shown in drawing 13.

[0132]Namely, in SOI substrate SB in the state (the state where MOS transistors Q31 and Q32 were formed in drawing 13 is illustrated) where even the trench isolation oxide film 16 was formed at least as shown in drawing 13, Resist mask RM3 is formed on the portion which does not pour in a logic section LP gas top and impurities, and impurities are poured in by ion implantation via the trench isolation oxide film 16. The dose is $1x10^{14}$-$1x10^{16}/cm^2$.

[0133]After it is not limited to a described method and forms the PG shield 103, before pouring of impurities forms the isolation oxide film 16, it may be performed, and the isolation oxide film 16 corresponding to the PG shield 103 top may be removed, and where SOI area 23 is exposed, it may be performed.
[0134]<C-4. modification 2> The PG shield 103A (shield layer) which formed the silicide film 33 in the upper part of each SOI area 23 may be used again like the semiconductor device 300A shown in drawing 14.
[0135]After forming the PG shield 103 shown in drawing 12, once covering the PG shield 103A with the isolation oxide film 16, it removes the isolation oxide film 16 corresponding to the PG shield 103 top, forms the opening 161, and exposes SOI area 23. Then, in the Salicide process for formation of MOS transistors Q31 and Q32 of logic section LP gas, the silicide film 33 is simultaneously formed on exposed SOI area 23. The opening 161 of the trench isolation oxide film 16 will be behind embedded with an interlayer insulation film.
[0136]Thus, since the PG shield 103A provided with the silicide film 33 on SOI area 23 serves as low resistance rather than the PG shield 103, an effect of prevention from an electrostatic induction loss increases.
[0137]As Embodiment 4 of a semiconductor device concerning <D. embodiment 4> <D-1. equipment configuration> this invention, composition of the semiconductor device 400 is shown in drawing 15.
[0138]The semiconductor device 400 shown in drawing 15 shows composition in which RF circuit section RP and logic section LP gas were allocated on SOI substrate SB like the semiconductor device 300 shown in drawing 12.
[0139]In RF circuit section RP, the PG shield 104 (shield layer) which comprises mutually close SOI areas 241-249 is formed in SOI layer 3 corresponding to region disposing of spiral inductor SI (plane constitution is referring to drawing 70).
[0140]Between RF circuit section RP and logic section LP gas, the trench isolation oxide film 15 which is a partial isolation oxide film is allocated, in logic section LP gas, with the trench isolation oxide film 15, SOI layer 3 is divided and SOI areas 71 and 72 are formed. And MOS transistors Q31 and Q32 are formed in SOI areas 71 and 72, respectively.
[0141]In addition, about the same composition as the semiconductor device 300 explained using drawing 12, the same numerals are attached and overlapping explanation is omitted.
[0142]SOI areas 241-249 which constitute the PG shield 104 are adjacent fields, they are constituted so that conductivity types of high impurity concentration or impurities may differ, respectively, and they are constituted so that an eddy current may be intercepted by PN junction.
[0143]In drawing 15, SOI areas 241-249, respectively A P^- (P type impurities are included in low concentration) field, They are a P^+ (P type impurities are included in high concentration) field, a P^- field, an N^+ (N type impurities are included in high concentration) field, a P^- field, a P^+ field, a P^- field, an N^+ field, and a P^- field.
[0144]Here, plane view shape of the PG shield 104 is shown in drawing 16. Although plane view shape of the PG shield 104 is the same as shape of the PG shield 101 explained using drawing 2 and explanation about shape is omitted, A point that a portion which was the trench isolation oxide film 11 serves as a SOI area in the PG shield 101 differs from a point that the silicide film 11 is not allocated, greatly. A section in a X-X line in drawing 16 corresponds to composition of the PG shield 104 shown in drawing 15.

[0145]In the PG shield 104, since reverse bias is given to a diode constituted by PN junction in order to intercept not composition with which all the SOI areas are grounded like the PG shield 101 but an eddy current, there are some which are connected to power supply potential (Vcc).

[0146]For example, in drawing 16, SOI areas 242 and 246 are connected to earth potentials, SOI areas 244 and 248 are connected to power supply potential, and SOI areas 241, 243, 245, 247, and 249 are grounded via an adjoining P^+ field. In the above explanation, although SOI areas 244 and 248 are connected to power supply potential, even if it includes composition connected to power supply potential in this way, PG shield (Perforated Ground Shield) is called for convenience. Also in other embodiments described below, this is the same.

[0147]Reverse bias is given to a diode which comprises SOI areas 242, 243, and 244, SOI areas 244, 245, and 246, and SOI areas 246, 247, and 248 by the connection which more than a <D-2. operation effect> explained, It is prevented that forward bias is carried out by counter-electromotive force which generates an eddy current, and an electrostatic induction loss can be reduced, without receiving an electromagnetic induction loss resulting from an eddy current.

[0148]Since the PG shield 104 sends current by electrostatic induction through a grounded P^+ field (low resistance area), [the shield] To say nothing of the ability to reduce an electrostatic induction loss, since the PG shield 104 is formed in SOI layer 3, a conductor layer new for formation of PG shield is unnecessary, and device structure does not become complicated.

[0149]Since the trench isolation oxide film 15 which is a partial isolation oxide film separates between elements in logic section LP gas, The potential of a channel forming region (body region) can be fixed through the well area WR of the lower part of the trench isolation oxide film 15, and various problems by a substrate floating effect can be prevented.

[0150]In the explanation beyond <the D-3. modification 1>, although the plane view shape of the PG shield 104 was explained as the same thing as the PG shield 101 explained using drawing 2, the shape where it explained using drawing 3 - drawing 7 may be used for it. However, the pouring states of the impurities of a SOI area will differ in that case.

[0151]Namely, if topmost SOI area 21A in right-hand side is made into a P^+ field toward drawing 3, [in the shape shown in drawing 3] The field (field which serves as the trench isolation oxide film 11 at drawing 3) between clockwise adjacent SOI areas 21A is made into a P^- field, Hereafter, an N^+ field, a P^- field, a P^+ field, and a P^- field can be formed in a clockwise rotation in order, an N^+ field can be connected to power supply potential, and the P^+ field can carry out reverse bias of the diode by grounding.

[0152]If topmost SOI area 21C in right-hand side is made into a P^+ field toward drawing 5, [in the shape shown in drawing 5] It is made into a P^- field between clockwise adjacent SOI areas 21C, Hereafter, an N^+ field, a P^- field, a P^+ field, and a P^- field can be formed in a clockwise rotation in order, an N^+ field can be connected to power supply potential, and the P^+ field can carry out reverse bias of the diode by grounding.

[0153]If topmost SOI area 21D is made into a P^+ field, for example, [in the shape shown in drawing 6] It is made into a P^- field between SOI areas 21D under it, and hereafter, an N^+ field, a P^- field, a P^+ field, and a P^- field can be formed in order, an N^+ field can be connected to power supply potential, and the P^+ field can

carry out reverse bias of the diode by grounding.

[0154]In shape shown in drawing 7, if SOI area 21E is made into a P^+ field, it will be made into a P^- field between SOI areas 21S, for example, SOI area 21S between an N^+ field and SOI areas 21S and 21M A P^- field, A P^- field and SOI area 21L can be made into an N^+ field between a P^+ field and SOI areas 21M and 21L, SOI area 21M can connect an N^+ field to power supply potential, and the P^+ field can carry out reverse bias of the diode by grounding.

[0155]In the PG shield 104 shown in <D-4. modification 2> drawing 15, although a SOI area of right and left of a low concentration impurity region (P^- field) had turned into a P^+ field and an N^+ field, it may use right and left of a low concentration impurity region as the same conductivity type.

[0156]That is, as shown in drawing 17 in which PG shield 104 portion is shown, SOI areas 242, 244, 246, and 248 are made into an N^- field, and it is good also considering all other fields as a P^+ field.

[0157][and a thing for which SOI areas 243 and 247 are connected to power supply potential, and SOI areas 241, 245, and 249 are grounded] A diode which comprises SOI areas 241 and 242, a diode which comprises SOI areas 248 and 249, Reverse bias is given to a diode which comprises SOI areas 245 and 246, and a diode which comprises SOI areas 244 and 245, It is prevented that forward bias is carried out by counter-electromotive force which generates an eddy current, and an electrostatic induction loss can be reduced, without receiving an electromagnetic induction loss resulting from an eddy current.

[0158]Since the number of times of superposition of an implanting mask decreases in the implantation process since the number of SOI areas is two sufficient, and a margin required for superposition of a mask can be made small, the miniaturization of the pattern of a SOI area can be carried out.

[0159]Although a SOI area was made into two kinds, an N^- field and a P^+ field, in the above explanation, it cannot be overemphasized that it is good also as two kinds, a P^- field and an N^+ field.

[0160]As Embodiment 5 of a semiconductor device concerning <E. embodiment 5> <E-1. equipment configuration> this invention, composition of the semiconductor device 500 is shown in drawing 18.

[0161]The semiconductor device 500 shown in drawing 18 shows the composition in which RF circuit section RP and logic section LP gas were allocated on SOI substrate SB like the semiconductor device 300 shown in drawing 12.

[0162]In RF circuit section RP, the PG shield 105 (shield layer) which comprises mutually close SOI areas 261-269 is formed in SOI layer 3 corresponding to the region disposing of spiral inductor SI (plane constitution is referring to drawing 70). And the PG shield 105 top is covered with the trench isolation oxide film 17 which is a partial isolation oxide film.

[0163]The trench isolation oxide film 17 extends to logic section LP gas, in logic section LP gas, with the trench isolation oxide film 15, SOI layer 3 is divided and SOI areas 71 and 72 are formed. And MOS transistors Q31 and Q32 are formed in SOI areas 71 and 72, respectively.

[0164]In addition, about the same composition as the semiconductor device 300 explained using drawing 12, the same numerals are attached and overlapping explanation is omitted.

[0165]SOI areas 261-269 which constitute the PG shield 105 are adjacent fields, they are constituted so that conductivity types of high impurity concentration or impurities may differ, respectively, and they are constituted so that an eddy current may be intercepted by PN junction.

[0166]In drawing 18, SOI areas 261-269, respectively A P^- field, A P^+ field, a P^- field, an N^+ field, a P^- field, It is a P^+ field, a P^- field, an N^+ field, and a P^- field, and connection with the plane view shape, power supply potential, and earth potentials and operation are the same as the PG shield 104 explained using drawing 15.

[0167]As shown, for example in drawing 18, [the connection with power supply potential and earth potentials] What is necessary is to provide contact part CP2 so that the interlayer insulation film 4 and the trench isolation oxide film 17 may be penetrated and SOI area 268 (N^+ field) may be arrived at, and just to connect wiring WL1 connected with power supply potential or earth potentials contact part CP2.
[0168]In the semiconductor device 500 which more than the <E-2. operation effect> explained, like the semiconductor device 400 explained using drawing 15, an eddy current can be intercepted in the PG shield 105, and the electromagnetic induction loss by an eddy current is not received.

[0169]Since the PG shield 105 sends the current by electrostatic induction through the grounded P^+ field (low resistance area), [the shield] To say nothing of the ability to reduce an electrostatic induction loss, since the PG shield 105 is formed in SOI layer 3, a conductor layer new for formation of PG shield is unnecessary, and device structure does not become complicated.
[0170]The trench isolation oxide film 17 can prevent a manufacturing process from being able to form simultaneously at a process of forming the trench isolation oxide film 15 in logic section LP gas, and becoming complicated since pouring of impurities to a SOI area is also easy.
[0171]Namely, [like / after forming at process same with having explained the trench isolation oxide films 15 and 17 using drawing 9 - drawing 11 / a process explained using drawing 13] From the upper part of the trench isolation oxide film 17, the PG shield 105 can be formed by carrying out the ion implantation of P type impurities and the N type impurities to a SOI layer of the trench isolation oxide film 17 lower part alternatively.
[0172]Since the trench isolation oxide film 15 which is a partial isolation oxide film separates between elements in logic section LP gas, Potential of a channel forming region (body region) can be fixed through the well area WR of the lower part of the trench isolation oxide film 15, and various problems by a substrate floating effect can be prevented.
[0173]Although the PG shield 105 top showed the composition covered with the trench isolation oxide film 17 which is a partial isolation oxide film in the semiconductor device 500 explained in the <F. embodiment 6> embodiment 5, Since PG shield is formed so that it may have an area equivalent to the allocation area of the plane direction of spiral inductor SI at least, it is necessary to form the trench isolation oxide film 17 over a large area.
[0174]In formation of a trench isolation oxide film, in forming a trench isolation oxide film over a large area although an unnecessary oxide film is removed by CMP treatment after embedding an oxide film at a trench, it becomes easy to generate here dishing to which the trench isolation oxide film concerned becomes depressed in dished.
[0175]The state where dishing occurred is shown in drawing 19. In drawing 19, the surface of the trench isolation oxide film 17A of a large area has become depressed in dished, and the trench isolation oxide film 15 of a narrow area is formed normally.
[0176]Unlike shape of a top edge part of a normal trench isolation oxide film, shape of a top edge part of a

trench isolation oxide film which dishing generated may affect the characteristics of an MOS transistor.
[0177]Composition which prevented generating of such dishing is explained in Embodiment 6 of a semiconductor device concerning this invention.
[0178]As Embodiment 6 of a semiconductor device concerning <F-1. equipment configuration> this invention, composition of the semiconductor device 600 is shown in drawing 20.
[0179]The semiconductor device 600 shown in drawing 20 shows composition in which RF circuit section RP and logic section LP gas were allocated on SOI substrate SB like the semiconductor device 300 shown in drawing 12.
[0180][in RF circuit section RP] [in SOI layer 3 corresponding to the region disposing of spiral inductor SI (plane constitution is referring to drawing 70)] The PG shield 106 (shield layer) which comprises the silicide film 34 formed on mutually close SOI areas 271-279, SOI areas 272, 274, and 276, and 278 is formed.
[0181]Here, SOI areas 271, 273, 275, 277, and 279 have thickness thinner than other SOI areas, and the trench isolation oxide film 18 which is a partial isolation oxide film is formed in the upper part. The trench isolation oxide film on SOI area 271 has extended to logic section LP gas.
[0182]And in logic section LP gas, with the trench isolation oxide film 15, SOI layer 3 is divided and SOI areas 71 and 72 are formed. And MOS transistors Q31 and Q32 are formed in SOI areas 71 and 72, respectively.
[0183]In addition, about the same composition as the semiconductor device 300 explained using drawing 12, the same numerals are attached and the overlapping explanation is omitted.
[0184]SOI areas 271-279 which constitute the PG shield 106 are adjacent fields, they are constituted so that the conductivity types of high impurity concentration or impurities may differ, respectively, and they are constituted so that an eddy current may be intercepted by PN junction.
[0185]In drawing 20, SOI areas 271-279, respectively A P^- field, It is an N^+ field, a P^- field, a P^+ field, a P^- field, an N^+ field, a P^- field, a P^+ field, and a P^- field, and the trench isolation oxide film 18 is formed on the P^- field.
[0186]Here, the plane view shape of the PG shield 106 is shown in drawing 21. The plane view shape of the PG shield 106 is the same as the shape of the PG shield 101 explained using drawing 2, and the explanation about shape is omitted. The section in the X-X line in drawing 21 corresponds to the composition of the PG shield 106 shown in drawing 20.
[0187]In drawing 21, since reverse bias is given to the diode constituted by PN junction in order to intercept an eddy current, SOI areas 272 and 276 are connected to power supply potential (Vcc), and SOI areas 274 and 278 are grounded.
[0188]In the semiconductor device 600 which more than the <F-2. operation effect> explained, since the trench isolation oxide film 18 with a narrow area is formed in the formation area of the PG shield 106, generating of dishing can be prevented.
[0189]In the PG shield 106, the electromagnetic induction loss by an eddy current can be reduced like the semiconductor device 400 explained using drawing 15.
[0190]Since the PG shield 106 sends the current by electrostatic induction through the grounded P^+ field (high resistance domain), [the shield] To say nothing of the ability to reduce an electrostatic induction loss, since the PG shield 106 is formed in SOI layer 3, a conductor layer new for formation of PG shield is

unnecessary, and device structure does not become complicated.

[0191]The trench isolation oxide film 18 can be simultaneously formed at the process of forming the trench isolation oxide film 15 in logic section LP gas, and since pouring of the impurities to a SOI area is also easy also for formation of the silicide film 34, it can prevent a manufacturing process from becoming complicated.

[0192]Namely, in the Salicide process for [after forming at the process same with having explained the trench isolation oxide films 15 and 18 using drawing 9 - drawing 11] formation of MOS transistors Q31 and Q32 of logic section LP gas, The silicide film 34 is simultaneously formed on the exposed SOI area, and the PG shield 106 can be formed in the formation area of the PG shield 106 by carrying out the ion implantation of P type impurities and the N type impurities alternatively.

[0193]Since the trench isolation oxide film 15 which is a partial isolation oxide film separates between elements in logic section LP gas, The potential of a channel forming region (body region) can be fixed through the well area WR of the lower part of the trench isolation oxide film 15, and various problems by a substrate floating effect can be prevented.

[0194]In the PG shield 106 of the semiconductor device 600 shown in <F-3. modification> drawing 20, although the SOI area of the right and left of a low concentration impurity region (P^- field) had turned into a P^+ field and an N^+ field, it may use the right and left of a low concentration impurity region as the same conductivity type.

[0195]As a modification of the semiconductor device 600, the semiconductor device 600A is shown in drawing 22. The PG shield 106A (shield layer) in drawing 22 makes SOI areas 271, 273, 275, 277, and 249 an N^- field, and makes all other fields the P^+ field.

[0196]Here, the plane view shape of the PG shield 106A is shown in drawing 23. The plane view shape of the PG shield 106A is the same as the shape of the PG shield 101 explained using drawing 2, and the explanation about shape is omitted. The section in the X-X line in drawing 23 corresponds to the composition of the PG shield 106A shown in drawing 22.

[0197]In drawing 23, since reverse bias is given to a diode constituted by PN junction in order to intercept an eddy current, SOI areas 272 and 276 are connected to a power supply (Vcc), and SOI areas 274 and 278 are grounded.

[0198]A diode which comprises connecting in this way in SOI areas 273 and 274, Reverse bias is given to a diode which comprises SOI areas 274 and 275, and a diode which comprises SOI areas 277 and 278, It is prevented that forward bias is carried out by counter-electromotive force which generates an eddy current, and an electrostatic induction loss can be reduced, without receiving an electromagnetic induction loss resulting from an eddy current.

[0199]Since the number of times of superposition of an implanting mask decreases in the implantation process since the number of SOI areas is two sufficient, and a margin required for superposition of a mask can be made small, the miniaturization of the pattern of a SOI area can be carried out.

[0200]Although a SOI area was made into two kinds, an N^- field and a P^+ field, in the above explanation, it cannot be overemphasized that it is good also as two kinds, a P^- field and an N^+ field.

[0201]In Embodiment 6 which more than the <G. embodiment 7> described, although the composition for preventing dishing of the trench isolation oxide film in PG shield formation area was shown, it may carry out like the composition of Embodiment 7 described below.

[0202]As Embodiment 7 of the semiconductor device concerning <G-1. equipment configuration> this invention, the composition of the semiconductor device 700 is shown in drawing 24. In drawing 24, only the composition of RF circuit section RP is shown for simplification.

[0203]In [as shown in drawing 24] RF circuit section RP, [in SOI layer 3 corresponding to the region disposing of spiral inductor SI (plane constitution is referring to drawing 70)] The PG shield 107 (shield layer) which comprises the silicide film 35 formed on mutually close SOI areas 281-287, SOI areas 282 and 284, and 286 is formed.

[0204]Here, SOI areas 281, 283, 285, and 287 have thickness thinner than other SOI areas, and the trench isolation oxide film 19 which is a partial isolation oxide film is formed in the upper part. SOI area 281 and the trench isolation oxide film 19 on 287 are formed more widely than other trench isolation oxide films 17.

[0205]And contact part CP3 allocated by penetrating the interlayer insulation film 4 is connected to SOI areas 282 and 284 and the silicide film 35 on 286, and the contact part concerned is connected to wiring WL2 which leads to grounding allocated on the interlayer insulation film 4.

[0206]In addition, about the same composition as the semiconductor device 300 explained using drawing 12, the same numerals are attached and overlapping explanation is omitted.

[0207][SOI areas 281-287 which constitute the PG shield 107] SOI areas 282, 284, and 286 turn into a P^+ field altogether, and SOI areas 281, 283, 285, and 287 are N^- fields, and it is constituted so that an eddy current may be intercepted by PN junction.

[0208]Here, plane view shape of the PG shield 107 is shown in drawing 25. Plane view shape of the PG shield 107 makes shape in which SOI area 28 (general term of SOI areas 282, 284, and 286) of a rectangle which has a silicide film opened a gap in mutually, and was allocated in the shape of a matrix, and the trench isolation oxide film 19 is allocated between each SOI area 28.

[0209]A section in a Y-Y line in drawing 25 corresponds to composition of the PG shield 107 shown in drawing 24, and wiring WL2 is allocated by L character type so that SOI area [which were allocated at intervals] 282 and 284 and 286 top may be followed.

[0210]Although wiring is allocated also on SOI area 28 of others which have a silicide film, except SOI area 28 of four corners, the wiring course is allocated so that it may become described [above] L character type, and, as for potential given to each wiring, earth potentials and power supply potential are given by turns.

[0211]Contact region CR for connecting a low concentration impurity region to power supply potential is allocated in a position distant from the PG shield 107.

[0212]A <G-2. operation effect> Reverse bias is given to all the diodes which comprise connecting in this way in a low-concentration SOI area and a high-concentration SOI area, It is prevented that forward bias is carried out by counter-electromotive force which generates an eddy current, and an electrostatic induction loss can be reduced, without receiving an electromagnetic induction loss resulting from an eddy current.

[0213]Since the PG shield 107 sends current by electrostatic induction through a grounded P^+ field (high resistance domain), [the shield] To say nothing of the ability to reduce an electrostatic induction loss, since the PG shield 107 is formed in SOI layer 3, a conductor layer new for formation of PG shield of that for which a process for formation of the wiring WL2 is needed is unnecessary, and device structure does not become complicated.

[0214]In the semiconductor device 700 which beyond the <G-3. modification 1> explained, although

composition which electrically connects a SOI area of the PG shield 107 by wiring WL2 was explained, a gate wire may be used like the semiconductor device 700A shown in drawing 26 instead of wiring WL2.

[0215]Namely, in the PG shield 107A (shield layer) of the semiconductor device 700A shown in drawing 26, On SOI areas 282 and 284 and 286, it does not have a silicide film, but the continuous gate wire GTL formed at the same process as the gate electrode of an MOS transistor has composition which touches SOI areas 282, 284, and 286 directly.

[0216]The insulating layer GZL formed at the same process as the gate dielectric film of an MOS transistor on the trench isolation oxide film 19 is allocated, and the silicide film GSL formed at the same process as the silicide film of an MOS transistor is allocated on the gate wire GTL.

[0217]The plane view shape of the gate wire GTL is allocated by L character type like wiring WL2 explained using drawing 25.

[0218]By having such composition, the manufacturing process of the wiring for electrically connecting a SOI area can be simplified.

[0219]<G-4. modification 2> Although the composition which intercepts an eddy current in the semiconductor device 700 again by PN junction between the SOI area covered with the trench isolation oxide film 19 which is a partial isolation oxide film, and the other SOI area was shown, It may be made to form the SOI area electrically separated completely using the complete isolation oxide film instead of the trench isolation oxide film 19 like the semiconductor devices 700B and 700C shown by drawing 27 and drawing 28.

[0220]The PG shield 107B (shield layer) of the semiconductor device 700B shown in drawing 27 is electrically separated completely by the trench isolation oxide film 191 which is a complete isolation oxide film.

[0221]The PG shield 107C (shield layer) of the semiconductor device 700C shown in drawing 28 is electrically separated completely by the trench isolation oxide film 192 which is a complete isolation oxide film.

[0222]Although it is the same, [in that the PG shield 107B and 107C separate a SOI area completely] In a logic section which is not illustrated, the trench isolation oxide film 192 can form between MOS transistors using a resist mask common when carrying out partial separation, and its new process cannot increase, and it can simplify a manufacturing method.

[0223]As Embodiment 8 of a semiconductor device concerning <H. embodiment 8> <H-1. equipment configuration> this invention, composition of the semiconductor device 800 is shown in drawing 29. The semiconductor device 800 shown in drawing 29 shows only composition of RF circuit section RP for simplification.

[0224]In [as shown in drawing 29] RF circuit section RP, SOI areas 291-299 which were mutually close in SOI layer 3 corresponding to region disposing of spiral inductor SI (plane constitution is referring to drawing 70), The PG shield 108 (shield layer) which comprises the silicide film 36 formed on SOI areas 291, 293, 295, and 297 and 299 is formed.

[0225]And false gate electrode MD1 which has the same section structure as a gate electrode of an MOS transistor is allocated in the upper part of SOI areas 292, 294, 296, and 298. False gate electrode MD1 has gate-dielectric-film DGZ, gate electrode DGT, the silicide film DGS, and the sidewall insulating layer DGW like an MOS transistor which is not illustrated.

[0226]The silicide film 36 is allocated on SOI areas 291, 293, 295, and 297 of the outside of the sidewall insulating layer DGW of false gate electrode MD1, and 299.

[0227]And SOI areas 291, 293, 295, 297, and 299 are N^+ fields, SOI areas 292, 294, 296, and 298 are P^- fields, SOI area 293 and the silicide film 36 on 297 are connected to power supply potential (Vcc), and SOI areas 291 and 295 and the silicide film 36 on 299, and the silicide film DGS on false gate electrode MD1 are grounded.

[0228]In addition, about the same composition as the semiconductor device 300 explained using drawing 12, the same numerals are attached and overlapping explanation is omitted.

[0229]Here, plane view shape of the PG shield 108 is shown in drawing 30. Although plane view shape of the PG shield 108 is the same as shape of the PG shield 101 explained using drawing 2 and explanation about shape is omitted, it differs greatly in that a portion which was the trench isolation oxide film 11 is false gate electrode MD1 in the PG shield 108. A section in a X-X line in drawing 30 corresponds to composition of the PG shield 108 shown in drawing 29.

[0230]In the PG shield 108, since reverse bias is given to a diode constituted by PN junction in order to intercept an eddy current, SOI areas 293 and 297 are connected to power supply potential, and SOI areas 291, 295, and 299 are grounded.

[0231]Since the lower part of the gate electrode DGT serves as a P^- field and the both sides serve as an N^+ field in false gate electrode MD1, are the so-called form of the N channel MOS transistor, but. A conductivity type is replaced and it cannot be overemphasized that it is good also as a form of a P channel MOS transistor. In that case, wiring to the power supply potential shown in drawing 30 and wiring to earth potentials will also be replaced.

[0232]The diode which comprises <H-2. operation effect> SOI areas 292 and 293, The diode which comprises SOI areas 293 and 294, the diode which comprises SOI areas 296 and 297, Reverse bias is given to the diode which comprises SOI areas 297 and 298, it is prevented that forward bias is carried out by the counter-electromotive force which generates an eddy current, and an electrostatic induction loss can be reduced, without receiving the electromagnetic induction loss resulting from an eddy current.

[0233]1st PG shield that comprises SOI areas 291-299 where the PG shield 108 is formed in SOI layer 3, and the silicide film 36, If it can distinguish to 2nd PG shield that comprises false gate electrode MD1 and 1st and 2nd PG shields are assumed to be resistance elements, respectively, it is connected in parallel between a parasitism capacitor and earth potentials, and these can reduce the resistance of PG shield further.

[0234]Although the composition which the lower part of the gate electrode DGT serves as a P^- field, and the both sides serve as an N^+ field in the PG shield 108 of the semiconductor device 800 which beyond the <H-3. modification> explained, and takes the form of an N channel MOS transistor was shown, In this case, since it operated as an MOS transistor when power supply potential was connected to the gate electrode DGT, had connected the gate electrode DGT to earth potentials, but. Since false gate electrode MD1 is not used as a gate electrode of an MOS transistor, the impurities pattern of the SOI area in SOI layer 3 is not limited to this.

[0235]For example, [like the PG shield 108A (shield layer) of the semiconductor device 800A shown in drawing 31] SOI areas 291, 295, and 299 are made into a P^+ field, SOI areas 292, 294, 296, and 298 are

made into a P^- field, and it is good also considering SOI areas 293 and 297 as an N^+ field.

[0236]And SOI areas 293 and 297 are connected to power supply potential (Vcc), SOI areas 291, 295, and 299 may be grounded, and the silicide film DGS of false gate electrode MD1 may be connected to the gate potential VGT.

[0237]While reverse bias is given to the diode which comprises a PN junction, and it is prevented that forward bias is carried out by the counter-electromotive force which generates an eddy current and being able to intercept an eddy current by connecting in this way, Even if it gives the gate potential VGT to the gate electrode DGT of false gate electrode MD1, it will not function as an MOS transistor, but the flexibility of selection of the potential of the gate electrode DGT of false gate electrode MD1 will increase.

[0238]Here, the plane view shape of the PG shield 108A is shown in drawing 32. The plane view shape of the PG shield 108A is the same as the shape of the PG shield 101 explained using drawing 2, and omit the explanation about shape, since potential arrangement is also explained using drawing 31, omit explanation, but. The section in the X-X line in drawing 32 corresponds to the composition of the PG shield 108A shown in drawing 31.

[0239]As Embodiment 9 of a semiconductor device concerning <I. embodiment 9> <I-1. equipment configuration> this invention, composition of the semiconductor device 900 is shown in drawing 33. The semiconductor device 900 shown in drawing 33 shows only composition of RF circuit section RP for simplification.

[0240]In [as shown in drawing 30] RF circuit section RP, SOI areas 291-299 which were mutually close in SOI layer 3 corresponding to region disposing of spiral inductor SI (plane constitution is referring to drawing 70), The PG shield 109 (shield layer) which comprises the silicide film 36 alternatively formed on SOI areas 291, 293, 295, and 297 and 299 is formed.

[0241]And SOI areas 291, 295, and 299 are P^+ fields, SOI areas 292, 294, 296, and 298 are P^- fields, SOI areas 293 and 297 are N^+ fields, SOI areas 293 and 297 are connected to power supply potential (Vcc) via the silicide film 36, and SOI areas 291, 295, and 299 are grounded via the silicide film 36.

[0242]In the PG shield 109, since reverse bias is given to a diode constituted by PN junction in order to intercept an eddy current, SOI areas 293 and 297 are connected to power supply potential, and SOI areas 291, 295, and 299 are grounded.

[0243]Here, plane view shape of the PG shield 109 is shown in drawing 34. Although plane view shape of the PG shield 109 is the same as shape of the PG shield 101 explained using drawing 2 and explanation about shape is omitted, it differs greatly in that a portion which was the trench isolation oxide film 11 serves as the silicide film 36 in the PG shield 109. A section in a X-X line in drawing 34 corresponds to composition of the PG shield 109 shown in drawing 33.

[0244]In addition, about the same composition as the semiconductor device 800A explained using drawing 31, the same numerals are attached and the overlapping explanation is omitted.

[0245]If the formation method of the <I-2. manufacturing method> PG shield 109 is explained briefly, first, a P type (or N type impurities) will be comparatively poured into low concentration, and a P^- layer (or N^- layer) will be formed in SOI layer 3. Next, using a resist mask, P type impurities are comparatively poured into high concentration, SOI areas 291, 295, and 299 which are P^+ fields are formed alternatively, and N type impurities are comparatively poured into high concentration, and SOI areas 293 and 297 which are N^+ fields

are formed alternatively. In this case, the field where neither of the impurities is poured into high concentration remains as a P^- field.

[0246]And as shown in drawing 35, silicide protection film PT is formed so that SOI areas 292, 294, 296, and 298 which are P^- fields may be covered.

[0247]A silicide protection film will cover the source drain area of the MOS transistor which inconvenience produces, if a silicide film is formed, is a film for preventing formation of a silicide film, and is formed by insulating layers, such as silicon oxide.

[0248]And it crosses to the whole surface and metal membrane MF, such as cobalt and titanium, is formed so that SOI areas 291, 293, 295, 297, and 299 may be covered, and let the metal membrane concerned be the silicide film 361 by a silicide reaction. And the silicide film 36 can be alternatively formed by removing unreacted metal membrane MF on silicide protection film PT.

[0249]Silicide protection film PT is forming so that it may be partially engaged also on the SOI area of both the sides of a P^- field, and can prevent the silicide film 36 from being formed on the SOI area of both the sides of a P^- field certainly.

[0250]Although the composition to which a SOI area is close similarly was shown in the PG shield 104 of the semiconductor device 400 explained using <I-3. operation effect> drawing 15, Since the diode by PN junction was no longer constituted when the silicide film was continuously formed on each SOI area, the composition which does not form a silicide film was shown. However, if it does not have a silicide film at all, it may be difficult to reduce the resistance of a SOI area, but in the PG shield 109, though discontinuous, since a silicide film is formed, the resistance of a SOI area can be reduced.

[0251]<I-4. modification> Although the conductivity type of the SOI area of both the sides of a P^- field showed mutually different composition in the PG shield 109 of the semiconductor device 900 explained above in addition, Like the PG shield 109A (shield layer) of the semiconductor device 900A shown in drawing 36, it is good also as the same in the conductivity type of the SOI area of both the sides of a low concentration field.

[0252]That is, in the PG shield 109A, SOI areas 292, 294, 296, and 298 are N^- fields, and SOI areas 291, 293, 295, 297, and 299 are all P^+ fields.

[0253]And SOI areas 291, 295, and 299 are grounded via the silicide film 36, and SOI areas 293 and 297 are connected to power supply potential (Vcc) via the silicide film 36.

[0254]It is prevented that forward bias is carried out by the counter-electromotive force which reverse bias is given [counter-electromotive force] to the diode constituted by PN junction, and generates an eddy current by having such composition, and an electrostatic induction loss can be reduced, without receiving the electromagnetic induction loss resulting from an eddy current.

[0255]Since the number of times of superposition of an implanting mask decreases in the implantation process since the number of SOI areas is two sufficient, and a margin required for superposition of a mask can be made small, the miniaturization of the pattern of a SOI area can be carried out.

[0256]Although a SOI area was made into two kinds, an N^- field and a P^+ field, in the above explanation, it cannot be overemphasized that it is good also as two kinds, a P^- field and an N^+ field.

[0257]As Embodiment 10 of a semiconductor device concerning <J. embodiment 10> <J-1. equipment

configuration> this invention, composition of the semiconductor device 1000 is shown in drawing 37.
[0258]In Embodiments 1-10 concerning this invention explained above, while preventing an electrostatic induction loss by a spiral inductor, explained composition of PG shield which prevents an electromagnetic induction loss by an eddy current in the inside, but. It may not generate only by a spiral inductor and an electrostatic induction loss may be generated also in a conductor wire formed in straight shape of metallic wiring etc., or a curve-like conductor wire. That is, if it is the composition of having not only an inductance element but an inductance and is, it has the same technical problem. This invention is applicable also to inductance elements other than a spiral inductor, and composition which has an inductance. Hereafter, composition which applies this invention as an example for prevention from an electrostatic induction loss by an inductance by straight shape wiring is shown.
[0259]In the semiconductor device 1000 shown in drawing 37, the PG shield 201 (shield layer) constituted by arranging conductor layer CL which carried out mutually-independent to the lower part of wiring WL3 along the arranged directions is allocated, and the electrostatic induction loss by wiring WL3 can be prevented by grounding conductor layer CL.
[0260]Here, an example of the section composition of the semiconductor device 1000 is shown to drawing 38. The semiconductor device 1000 shown in drawing 38 shows only the composition of RF circuit section RP, if the semiconductor device 90 explained using drawing 68 is taken for an example.
[0261]In SOI substrate SB which comprises the silicon substrate 1, the embedded oxide film 2 allocated on this silicon substrate 1, and SOI layer 3 allocated on the embedded oxide film 2 in drawing 38, The field corresponding to the region disposing of wiring WL3 of SOI layer 3 is divided by two or more trench isolation oxide films 13, and two or more SOI areas 22 are formed. The trench isolation oxide film 12 is formed by embedding silicon oxide in the trench allocated so that the surface of the embedded oxide film 2 might be arrived at from the surface of SOI layer 3, and each SOI area 22 is separated completely electrically.
[0262]The silicide film 32 is allocated in the upper part of each SOI area 22, and the PG shield 201 is constituted by two or more trench isolation oxide films 13, SOI area 22, and the silicide film 32, respectively. A cascade screen which comprises SOI area 22 and the silicide film 32 corresponds to conductor layer CL shown in drawing 37.
[0263]SOI area 22 and plane view shape of the silicide film 32 are rectangles which extend crosswise [of wiring WL3], as are shown in drawing 37 and it is certainly formed in the lower part of the cross direction of wiring WL3.
[0264]Here, although an eddy current in PG shield by a spiral inductor is generated in a field parallel to the principal surface of a semiconductor substrate, an eddy current by straight shape wiring WL3 is generated in a perpendicular field to a semiconductor substrate, as a dashed line shows drawing 37. Therefore, the thinner one of thickness of conductor layer CL is good, and makes it at least smaller than the length of the transverse direction of conductor layer CL.
[0265]The length of a longitudinal direction of conductor layer CL and a conductor layer CL allocation gap are set as about 1-3 micrometers.
[0266]Section composition of the PG shield 201 shown in drawing 38 is an example, and is not limited to this composition.
[0267]Since it has the PG shield 201 constituted in the semiconductor device 1000 by arranging conductor layer CL which carried out mutually-independent to the lower part of wiring WL3 along the arranged

directions as more than a <J-2. operation effect> explained, an electrostatic induction loss by wiring WL3 can be prevented.

[0268]Since the PG shield 201 is formed in SOI layer 3, a conductor layer new for formation of PG shield is unnecessary, and device structure does not become complicated.

[0269]A <J-3. modification> It is also effective to constitute conductor layer CL from a conductor film and a multilayer film of an insulating layer as composition for preventing again an eddy current generated in a perpendicular field to a semiconductor substrate in conductor layer CL.

[0270]That is, conductor layer CL1 is formed like the semiconductor device 1001 shown in drawing 39 with a multilayer film which allocated conductor film CF and the insulating layer ZF by turns in SOI layer 3.

[0271]And electric connection of each conductor film CF is made by contact part CP4 which penetrates SOI layer 3 and conductor layer CL1, and contact part CP4 is formed on SOI layer 3, and it is connected to wiring WL4 connected with earth potentials.

[0272]By such composition, an eddy current generated in a perpendicular field to a semiconductor substrate in conductor layer CL1 can be intercepted by the insulating layer ZF, and does not receive an electromagnetic induction loss by an eddy current.

[0273]Supperlattice structure of a conductor and an insulator may use a superlattice film laminated by turns instead of a multilayer film.

[0274]In Embodiments 1-10 which more than <K. embodiment 11> described, In a semiconductor device formed on a SOI substrate, while preventing an electrostatic induction loss by a spiral inductor or wiring, explained composition of PG shield which prevents an electromagnetic induction loss by an eddy current generated in the inside, but. Application of this invention is not limited to a SOI substrate, and can also be applied to a silicon substrate called a bulk board.

[0275]As Embodiment 11 of a semiconductor device concerning <K-1. equipment configuration> this invention, composition of the semiconductor device 2000 is shown in drawing 40. The semiconductor device 2000 shown in drawing 40 shows only composition of RF circuit section RP, if the semiconductor device 90 explained using drawing 68 is taken for an example.

[0276]In drawing 40, a field corresponding to region disposing of spiral inductor SI (plane constitution is referring to drawing 70) of the silicon substrate 1 of a P type is divided by two or more trench isolation oxide films 111, and two or more impurity ranges 121 where P type impurities were comparatively poured into high concentration (P^+) are formed.The trench isolation oxide film 111 is formed by embedding silicon oxide in a trench allocated so that a prescribed depth might be reached from the surface of the silicon substrate 1.

[0277]And N type impurities are the lower part of the impurity range 121 with the well area NW comparatively poured into low concentration (N^-).

[0278]The silicide film S131 is allocated in the upper part of each impurity range 121, and the PG shield 301 (shield layer) is constituted by two or more trench isolation oxide films 111, the impurity range 121, and the silicide film 131, respectively.

[0279]In addition, about the same composition as the semiconductor device 100 shown in drawing 1, the same numerals are attached and overlapping explanation is omitted.

[0280]Section composition shown in drawing 40 is an example, is not limited to this composition and can apply composition of various kinds of PG shields explained in Embodiments 1-10.

[0281][forming a low concentration well area into a substrate, and forming PG shield on it, as more than a <K-2. operation effect> explained] It becomes instead of a low concentration well area of high resistance being an embedded oxide film, and the impurity range 121 can be separated electrically mutually, and while being able to prevent an electrostatic induction loss also in a bulk board, PG shield which does not receive an electromagnetic induction loss by an eddy current can be obtained.

[0282]In Embodiments 1-11 which more than <L. embodiment 12> described, while preventing an electrostatic induction loss by a spiral inductor or wiring, explained composition of various PG shields which prevent an electromagnetic induction loss by an eddy current generated in the inside, but. An electromagnetic induction loss by a spiral inductor or wiring may occur [be / it / under / semiconductor substrate / of the lower part of these PG shields / also setting]. Hereafter, composition which prevents an electromagnetic induction loss in a semiconductor substrate is explained.

[0283]As Embodiment 12 of the semiconductor device concerning <L-1. equipment configuration> this invention, the composition of the semiconductor device 3000 is shown in drawing 41.

[0284]If the semiconductor device 90 explained using drawing 68 is taken for an example, the semiconductor device 3000 shown in drawing 41 shows a part of RF circuit section 91 and logic section 92, and shows it as RF circuit section RP and logic section LP gas, respectively.

[0285]In drawing 41, RF circuit section RP and logic section LP gas are allocated on SOI substrate SB which comprises the silicon substrate 1, the embedded oxide film 2 allocated on this silicon substrate 1, and SOI layer 3 allocated on the embedded oxide film 2.

[0286]In RF circuit section RP, a field corresponding to region disposing of spiral inductor SI (plane constitution is referring to drawing 70) of SOI layer 3 is divided by two or more trench isolation oxide films 13, and two or more SOI areas 22 are formed. And the silicide film 32 is allocated in the upper part of each SOI area 22, and the PG shield 102 is constituted by two or more trench isolation oxide films 13, SOI area 22, and the silicide film 32, respectively.

[0287]And the hollow part CV is allocated in an inside of the silicon substrate 1 of the lower part of the PG shield 102.

[0288]The hollow part CV has the depth (it is about 100 micrometers at the maximum) comparable as the length of a plane direction of spiral inductor SI, and a spread of a plane direction is set up to include a formation area of spiral inductor SI at least.

[0289]And the embedded oxide film 2, SOI layer 3, the interlayer insulation films 4 and 5, and the opening OP that penetrates the wrap insulating layer 6 and reaches the hollow part CV in spiral inductor SI are allocated.

[0290]In addition, the same numerals are attached about the same composition as the semiconductor device 200 explained using drawing 8, and explanation is omitted.

[0291]After the formation method of the hollow part CV forms the composition to insulating layers 6 other than the hollow part CV on SOI substrate SB, The opening OP which reaches the silicon substrate 1 is formed, for example, the 20% solution of KOH (potassium hydrate) is poured in from the opening OP, and the method of etching the silicon substrate 1 can be taken. Eventually the lower part OP is embedded by an insulating layer etc.

[0292]Other solution may be sufficient as long as it is solution which is not limited to KOH solution as an etching solution, and melts only a silicon substrate. For example, strong alkali solutions, such as NaOH, are

also usable. Although it needs to be cautious of contamination of potassium (K) and sodium (Na), since it is a simple substance, it is easy to treat such solution. Organic substances, such as catechol ($C_6H_6O_2$) and TMAH (water oxidization tetramethylammonium: $N(CH_3)_4OH$) solution, may be used. Which solution is used should just choose to compensate for the composition of the whole chip fabrication factory which performs device fabrication. Etching solutions, such as KOH solution, differ in an etching rate with temperature, and the 20% solution of KOH has an etching rate of 100 nm/min at 50 **.

[0293]On SOI substrate SB, the hollow part CV may be formed in the state of forming nothing, may be formed in the stage in which even the PG shield 102 was formed, and may be fundamentally formed in any stage.

[0294]Since the semiconductor device 3000 has the hollow part CV inside the silicon substrate 1 of the lower part of the PG shield 102 as more than the <L-2. operation effect> explained, While preventing the electrostatic induction loss by a spiral inductor with the PG shield 102, the electromagnetic induction loss by the eddy current generated inside the PG shield 102 is not received.Within the silicon substrate 1, generating of the eddy current by spiral inductor SI can be prevented, and an electromagnetic induction loss can be reduced.